UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/478,122	01/05/2000	Laurence A. Thompson	DVDOP015	1276

7590   10/09/2003

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EXAMINER
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ART UNIT	PAPER NUMBER
2643	5

DATE MAILED: 10/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _05 January 2000_ .

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-34_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-34_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4)☐ Interview Summary (PTO-413) Paper No(s). _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: .

DETAILED ACTION

Introduction

1.   Claims 1-34 of U.S. application 09/478,122 filed on 01/05/2000 are presented for

examination.

Claim Objections

2.   Claim 21 is objected to because of the following informalities: claim 21 recites "22"

on line 1, which appear to be --- 20---. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed
> publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1 and 20 are rejected under 35 U.S.C. 102(a) as being anticipated by

applicant's specification.

Consider claim 1 applicant's prior art teaches an apparatus for delaying an audio

signal comprising:

an input device (see fig.1 (input))receptive to an audio signal having one of a plurality

of formats (A, B, C, format);

a processing device (provide delay of (X Y Z)) coupled to the input device, the

processing device configured for providing a delay in the audio signal corresponding to

the format of the audio signal; and

an output device (see fig.1 (output)) coupled to the processing device, the output

device configured to output the audio signal with the delay corresponding to the format

of the audio signal (see specification page 2-3).

As to claim 20, there is the method claim corresponding to apparatus claim 1, see

previous apparatus claim 1 rejection.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by
> another filed in the United States before the invention by the applicant for patent or (2) a patent
> granted on an application for patent by another filed in the United States before the invention by the
> applicant for patent, except that an international application filed under the treaty defined in section
> 351(a) shall have the effects for purposes of this subsection of an application filed in the United States
> only if the international application designated the United States and was published under Article 21(2)
> of such treaty in the English language.

4.   Claims 1-7, 20-21 and 23-25, are rejected under 35 U.S.C. 102(e) as being

anticipated by Sueyoshi (US PAT 6,233,562).

Consider claim 1, Sueyoshi teaches an apparatus for delaying an audio signal

comprising:

An input device (see fig.1, bit stream) receptive to an audio signal having one of a

plurality of formats (such as MPEG1 OR MPEG2 and see col.4 lines 3-6);

A processing device (1, 2) coupled to the input device (bit stream), the processing

device configured (1,2) for providing a delay (such as channel A to be reproduced at

time t=t0 is inserted into an area 2-8, and a coded signal to be reproduced at time t=t1

is inserted into a area 2-10 (see fig.2) and channel B reproduced at time t=t0 is inserted

into an area 2-9, and a coded signal to be reproduced at time t=t1 inserted into area 2-9

(see fig.2)) and inherently the audio signal corresponding to the format of the audio

signal (see col.4 line 43-col.5 line29); and

an output device (3) coupled to the processing device (12), the output device (3)

configured to output the audio signal with the delay corresponding to the format of the

audio signal (see col.5 line 48-col.6 line 26).

Consider claim 20, there is the method claim corresponding to apparatus claim1,

See previous apparatus claim 1 rejection.

Consider claims 2-3, Sueyoshi teaches the apparatus of the audio signal further

comprises inherently a serial audio clock signal (to synchronize an audio signal output

from the internal decoder and an audio signal out put from the external, it needs a clock

cycle to control it) and a plurality of accompanying signals (see col.2 line 25- 59); and

the accompanying signals further comprises a data signal and a frame synchronization

signal (see col.2 lines 25-59).

As to claims 21 and 23, these are the method claims of claims 2-3 respectively. Thus

note claims 2-3, respectively for rejection.

Consider claims 4-7, Sueyoshi teaches the apparatus of the accompanying signals

are loaded into a register (see fig.1, (1 and 3); and the register is a FIFO register (col.5

lines 19-29); and the accompanying signals are stored in a memory device (see fig.1 (1

and 3)); and the memory device further comprises a memory controller (DSP) and a

memory chip (DRAM and see col.6 line 33 –63).

As to claims 24-25, these are the method claims of claims 6-7 respectively. Thus

note claims 6-7, respectively for rejection.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 8-19, 22 and 25-34 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Sueyoshi (US PAT 6,233,562) in view of Kuwaoka (US PAT.

6,449,519).

Consider claim 8, Sueyoshi does not teaches clearly the apparatus of the

processing device further comprises an audio format detection device operable to

detect the format of the audio signal (see fig.15).

However, Kuwaoka teaches the apparatus of the processing device further

comprises an audio format (formation) detection device (see fig.3, (28,25) operable to

detect the format (formation) of the audio signal 9see col.8 line 51-col.9 line 6).

Therefore, it would obvious to one of ordinary skill in the art at the time invention was made to combine the teaching of Sueyoshi into Kuwaoka to provide a compact and high-performance audio information processing apparatus.

Consider claim 26, there is the method claim corresponding to apparatus claim 8, See previous apparatus claim 8 rejection.

Consider claims 9-11, Kuwaoka teaches the apparatus of the audio format (formation) detection device (see fig.3, (25,28)) is operable to detect a number of edge (top peak A1 and under peak B1) transitions in the serial audio clock signal (timing control) and provide a corresponding detected count (28 and 25i)(see col.9 line 55-col.10 line 50); and the apparatus of the audio format (formation) detection device (28,25i) further comprises a plurality of model data (25-25h), wherein each model data represents one of the plurality of audio signal formats (formations) and a corresponding one of a plurality of delay data, wherein the detected count (28,25i) is compared (23,24) to the model data, the audio format (formation) detection device (25i,28) operable to provide the delay data representing the model data that is equal to the detected count (see col.8 line 28-col.9 line 50); and the apparatus of the processed clock signal is synchronized (by timing control circuit) inherently to a reference clock (see col.8 line 51-col.9 line 6).

As to claims 27-28, these are the method claims of claims 9-10 respectively. Thus note claims 9-10, respectively for rejection.

Consider claim 12 Sueyoshi teaches the apparatus of the audio format (frame data) detection device is inherently operable to provide a processed clock signal by dividing

the serial audio clock signal by a constant (such as each frame fk (k=1, 2, 3..)(see

col.13 line 60-col.14 line 22).

Consider claim 22, there is the method claim corresponding to apparatus claim 12,

See previous apparatus claim 12 rejection.

Consider claims 13-14 and 17-18, Kuwaoka teaches the apparatus of the

processing device is operable to compare a new delay data (current audio data) to an

old delay data (audio data of a before), the processing device operable to reconfigure a

buffer if the new delay data is not equal to the old delay data (see col.9 line 17-35); and

the apparatus of the detected count is compared to the model data by a plurality of

comparators (see fig.3, (23,24) and col.9 line 17-57); and the apparatus of the

processing device further comprises a memory unit (see fig.3, 25) to provide the delay

corresponding to the delay data (see col.8 lines 27-65); and the apparatus of the

processing device further comprises a first parameter and a second parameter, the first

parameter configured according to the provided delay data.

Consider claim 29, there is the method claim corresponding to apparatus claim 14,

See previous apparatus claim 14 rejection.

Consider claims 15-16 Sueyoshi teaches the apparatus of the provided delay data

is a first offset value (see fig.1 4a, sent by pointer controller), the processing device

operable to resize a write address pointer (actual pointer and temporary pointer) with

the offset value (sent by pointer controller, 4a and see col.4 lines 2-42); and the

apparatus of the provided delay data is a second offset value (sent by pointer controller,

4a), the processing device operable to resize a read address pointer (actual pointer and

temporary pointer) with the offset value (sent by pointer controller, 4a and see col.4

lines 2-42).

Consider claims 18-19, Sueyoshi teaches apparatus of the processing device (see

fig.1, 2) further comprises a first parameter (write = replace information) and a second

parameter (read information), the first parameter configured inherently according to the

provided delay data (see col.4 lines 2-44); and the apparatus of the first parameter

(information) is a write address parameter (actual pointer and temporary pointer), the

second parameter (information) is a read address parameter (actual pointer and

temporary pointer), and the memory unit is a buffer (see col.4 lines 2-44).

Consider claim 22, Sueyoshi teaches the method of the step of processing the

audio signal further comprises the step of providing inherently a processed serial audio

clock signal, the processed serial audio clock signal provided by dividing the serial

audio clock signal (such as each frame fk (k=1,2, 3.... Constant) by a constant (see

col.13 line 60-col.14 line4).

Consider claims 30-31, Sueyoshi teaches the method of the detected count further

comprises the number of edge (border) transitions in the processed inherently serial

audio clock signal within a period (each frames), and wherein the plurality of model data

include the number of edge (border) transitions present in each processed serial audio

clock signal format in the period (each frames and see col.13 line 60-col.14 line 43) and

the method of the step of processing the audio signal further comprises the step of

providing a memory register (see fig.1, (1,2,,3) having a first parameter (actual pointer

for replace information) and a second parameter (actual pointer for reading information), the memory register inherently configured to provide a delay (see col.4 lines 3-43).

Consider claims 32-34, Sueyoshi teaches the method of the step of providing a memory register (see fig.1, (1,2, 3)) further comprises the step of providing an offset (4a, pointer controller), the offset corresponding to inherently the model data equal to the detected count and resizing the memory register by providing the offset (pointer controller) for the first parameter (replaced with information)(see col.4 lines 2-44); and the method of the first parameter (replaced with information) is a write address pointer(actual pointer and temporary pointer), the second parameter (reading information) is a read address pointer (actual pointer and temporary pointer), and the memory register is a buffer (see col.4 lines 2-42); the method of the first parameter (reading information) is a read address pointer(actual pointer and temporary pointer), the second parameter (replaced with information) is a write address pointer(actual pointer and temporary pointer), and the memory register is a buffer (see col.4 lines 2-42).

Conclusion

7.   The prior art of record and not relied upon is considered pertinent to applicant's disclosure. Kuroda (US PAT 6,501,904) and Lee (US PAT 6,430,361) are recited to show other related the audio signal delay apparatus and method.

8.   Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington.

VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Lao,Lun-See whose telephone number is (703) 305-2259 The examiner

can normally be reached on Monday-Friday from 8:00 to 6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Curtis Kuntz, can be reached on (703) 305-4708.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the Technology Center 2600 whose telephone number is (703) 306-0377.

Lao,Lun-See
Patent Examiner
US Patent and Trademark Office
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(703305-2259

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PRIMARY EXA!